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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/918,604	07/30/2001	Haneef D. Mohammed	CYPR-CD01057	5237

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EXAMINER	
DO, CHAT C	

ART UNIT	PAPER NUMBER
2193	

DATE MAILED: 05/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/918,604	MOHAMMED ET AL.	
	Examiner	Art Unit	
	Chat C. Do	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 17 November 2004.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-19 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-19 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is responsive to Amendment filed 11/17/2004.

2. Claims 1-19 are pending in this application. Claims 1, 8 and 16 are independent claims. This Office action is made final.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

4. Claims 1-19 are rejected under 35 U.S.C. 102(a) as being anticipated by Kobayashi et al. (U.S. 6,199,091).

Re claim 1, Kobayashi et al. disclose in Figures 1-2 a method of performing a pipelined arithmetic function (wherein Figure 2 is an extension of Figure 1) comprising the steps of:

a) receiving two N-bit operands (e.g. X and Y are two N-bit operands) into each of a plurality of adder elements in separate pipelines (e.g. first adder yields Z0-Z2 and second adder yields Z3-Z8 in separate pipelines),

b) performing an add operation in each of plurality of adder elements wherein a first N-bit result (e.g. Z0-Z2) and a first carry bit (e.g. C1) is output from each of adder elements;

c) receiving first N-bit result from each of adder elements into a respective N-bit result register (e.g. registers to store the results for Z0-Z2) and receiving first carry bit from each of adder elements into a respective carry bit register (e.g. C1);

d) outputting from an incrementor (e.g. all the logics in the lower portion of producing Z3-Z4 except 7 and 9) in one of pipelines, a second N-bit result (e.g. Z3-Z4) and a second carry bit (e.g. C2) from the combination of a first result from a first of N-bit result registers (e.g. C1), a first carry bit from a first of carry bit registers (e.g. C1 from previous adder), and a first carry bit from a second of carry bit registers from a second of pipelines (e.g. second output line of 9); and

e) supplying a final result (e.g. Z3-Z8 for 9 bits) being a combination of second N-bit result from incrementor (e.g. C2 inputs into the next stage for computing Z5-Z8), second carry bit from incrementor, and first N-bit result (e.g. outputs of 13 and 17) from a second N-bit result register in second pipeline.

Re claim 2, Kobayashi et al. further disclose in Figures 1-2 the N-bit result registers are single width registers (e.g. non-register is double width).

Re claim 3, Kobayashi et al. further disclose in Figures 1-2 the carry bit registers are single bit registers (e.g. C1, C2, C3...).

Re claim 4, Kobayashi et al. further disclose in Figures 1-2 the step c) further comprises respectively receiving first N-bit result into a plurality of single width N-bit registers (e.g. box 7 it combines X3 and Y3 to yield a single bit result Z3).

Re claim 5, Kobayashi et al. further disclose in Figures 1-2 the step c) further comprises respectively receiving first carry bit into a plurality of single bit register (e.g. C1 is a single bit).

Re claim 6, Kobayashi et al. further disclose in Figures 1-2 the step d) further omprises respectively receiving second N-bit result into a plurality of single width N-bit registers (e.g. result of operands X,Y from 0-2 is Z0 to Z2).

Re claim 7, Kobayashi et al. further disclose in Figures 1-2 the step d) further comprises receiving second carry bit into a plurality of single bit registers (e.g. C2 is a single bit).

Re claim 8, it is an adder claim of claim 1 which has similar limitations. Thus, claim 8 is also rejected under the same rationale as cited in the rejection of rejected claim 1.

Re claim 9, it is an adder claim of claim 2 which has similar limitations. Thus, claim 9 is also rejected under the same rationale as cited in the rejection of rejected claim 2.

Re claim 10, it is an adder claim of claim 3 which has similar limitations. Thus, claim 10 is also rejected under the same rationale as cited in the rejection of rejected claim 3.

Re claim 11, it is an adder claim of claim 4 which has similar limitations. Thus, claim 11 is also rejected under the same rationale as cited in the rejection of rejected claim 4.

Re claim 12, it is an adder claim of claim 2 which has similar limitations. Thus, claim 12 is also rejected under the same rationale as cited in the rejection of rejected claim 2.

Re claim 13, it is an adder claim of claim 6 which has similar limitations. Thus, claim 13 is also rejected under the same rationale as cited in the rejection of rejected claim 6.

Re claim 14, it is an adder claim of claim 2 which has similar limitations. Thus, claim 14 is also rejected under the same rationale as cited in the rejection of rejected claim 2.

Re claim 15, Kobayashi et al. further disclose in Figures 1-2 a plurality of carry bit registers for respectively receiving carry bits from adder elements and incrementor (e.g. C1 from the first set of adder (1,3,5), C2 from the second set of adder(7,9) and incrementor (e.g. other lower portion of logics).

Re claim 16, it is a multistage adder claim of claim 1 which has similar limitations. Thus, claim 16 is also rejected under the same rationale as cited in the rejection of rejected claim 1.

Re claim 17, it is a multistage adder claim of claim 2 which has similar limitations. Thus, claim 17 is also rejected under the same rationale as cited in the rejection of rejected claim 2.

Re claim 18, it is a multistage adder claim of claim 6 which has similar limitations. Thus, claim 18 is also rejected under the same rationale as cited in the rejection of rejected claim 6.

Re claim 19, it is a multistage adder claim of claim 15 which has similar limitations. Thus, claim 19 is also rejected under the same rationale as cited in the rejection of rejected claim 15.

Response to Arguments

5. Applicant's arguments filed 11/17/2004 have been fully considered but they are not persuasive.

a. The applicant argues in page 9 for independent claims that the cited reference by Kobayashi et al. do not disclose a step of receiving two N-bit operands into each of a plurality of adder elements in separate pipelines.

The examiner respectfully submits that Figures 1-2 of cited reference clearly disclose a step of receiving two N-bit operands into each of a plurality of adder elements in separate pipelines as cited in the above rejection. In particular, the examiner interprets the first pipeline as receiving bits[1:2], the second pipeline as receiving bits[3:4], the third pipeline as receiving bits[5:8], and so on. Each of these pipelines includes an adder (e.g. first couple square boxes in the beginning stage) and a carry (e.g. C1 ...). Thus, each adder (e.g. {3,5}, {7,9}...) in each pipeline in Figures 1-2 receiving two-bits operands as cited in the claims.

b. The applicant argues in page 10 for independent claims that the cited reference by Kobayashi et al. do not disclose a step of performing an add operation in each of plurality

of adder elements wherein a first N-bit result and a first carry bit is output from each of adder elements.

As clearly stated above, each adder (e.g. {3,5}, {7,9}, {11,13}...) receives 2-bits operand (e.g. [1:2], [3:4], [5:6]...respectively), generate 2-bits result (e.g. {Z1:Z2}, {Z3:Z4}, {Z5:Z6}...respectively), and generate a carry out signal (e.g. the carry bit is the second pin from the second box of the adder (e.g. second output of each boxes 5, 9, 13...respectively).

c. The applicant argues in page 11 for independent claim that the cited reference by Kobayashi et al. do not disclose a step of receiving first N-bit result from each of adder elements into a respective N-bit result resister and receiving first carry bit from each of adder elements into a respective carry bit register;

Inherently and obviously, there must a register to store the result output once the adder completed for further processing and a carry bit register for crossing one pipeline to another pipeline.

d. The applicant argues in page 12 for independent claim that the cited reference by Kobayashi et al. do not disclose a step of outputting from an incrementor in one of pipelines.

The examiner interprets the portion in each pipeline which has the carry input from the previous adder as the incrementor. For instant, the logic gates 35, 33, 37, 41, and 43 combine as a logical incrementor.

e. The applicant argues in page 13 for claim 17 that the cited reference by Kobayashi et al. do not disclose clock regulated stages are used in any manner.

The examiner respectfully submits that there must be a clock to synchronize and regulate every pipeline stages by well known as clearly cited in the applicant argument. Therefore, the Figures 1-2 must have an operated clock to receiving N-bit operands, processing/adding, and generate output in a predetermined time manner.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (571) 272-3721. The examiner can normally be reached on M => F from 7:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaki Kakali can be reached on (571) 272-3719. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do
Examiner
Art Unit 2193

April 7, 2005